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EXAMINER

PERALTA, GINETTE

ART UNIT PAPER NUMBER

2814

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/683,328

Examiner

Ginette Peralta

Applicant(s)

FRIED ET AL.

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 20-28 is/are pending in the application.
- 4a) Of the above claim(s) 1-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 12-18, 20-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

*Election/Restrictions*

1. Claims 1-11 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

*Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 12-28 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a patterned stack including a vertical semiconductor body, does not reasonably provide enablement for exposed sidewalls, and a gate dielectric located on exposed sidewalls. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. In the instant case, claims 12-28 have the recited limitations of "a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate; a gate dielectric located on each exposed sidewall of said vertical semiconductor body", it is noted that since a gate dielectric is located on the sidewalls

of the semiconductor body, and that since the claims are directed to a structure and not a method wherein a gate dielectric may be formed on exposed areas, that the limitation of "exposed sidewalls" is not enabled in the structure when in the same claim another layer is covering the sidewalls.

4. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no enablement in the specification or the drawings for the claimed feature of the p-type gate portion, the n-type gate portion, the interconnect, and the planarizing structure having a same final shape, as it is shown in Figs. 5B, 6B, 7B, 8B, and 9B, the p-type gate portion and the n-type gate portion have a similar final shape, but the planarizing structure has a different final shape, and the interconnect has also different shape, thus the limitation is not reasonably conveyed in the specification.

*Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in-  
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application

published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 12, 19-27 are rejected under 35 U.S.C. 102(e) as being anticipated by

Enders et al. (U. S. Pat. 6,503,784 B1).

Regarding claim 12, Enders et al. discloses in Figs. 2S and 5C a field effect transistor that comprises a patterned stack including at least a vertical semiconductor body 54a having sidewalls 52 located on an upper surface of a substrate; a gate dielectric 52 located on the sidewalls of the vertical semiconductor body; a p-type gate portion 56p located on one side of the vertical semiconductor body and an n-type gate portion 56n located on an opposing side of the vertical semiconductor body 54a, the gate portions located on the upper surface of the substrate and are separated from the vertical semiconductor body 54a by the gate dielectric, and an interconnect located at least over the p-type gate portion and the n-type gate portion and a planarizing structure (110 and metal 1) above the interconnect 1.

Regarding claim 20, Enders et al. discloses the semiconductor body having a hard mask 57 present on an upper surface.

Regarding claim 21, Enders et al. discloses the hard mask comprising an oxide (col. 5, ll. 57-60).

Regarding claim 22, Enders et al. discloses that the n-type gate portion is comprised of N-doped polysilicon and the p-type gate portion is comprised of P-type polysilicon (col. 7, ll. 8-51, col. 8, ll. 1-16).

Regarding claims 23 and 24, Enders et al. discloses in Fig. 20 that the substrate comprises an upper insulating portion 80 and a lower semiconducting portion 14.

Regarding claim 25, Enders et al. discloses in Fig. 5C that part of the planarizing material is METAL 1.

Regarding claim 26, Enders et al. discloses source/drain regions in areas adjacent to the vertical semiconductor body (3D, 6D, 6S, etc.).

Regarding claim 27, Enders et al. discloses that the source/drain regions are doped so as to have either donor or acceptor impurities.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 14-18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enders et al..

Regarding claims 14, 15, and 18, Enders et al. discloses that the p-type gate portion and the n-type gate portion are composed of a polysilicon containing material.

Enders et al. further discloses that the planarizing structure comprises silicon oxide. Thus, although a different material, silicon oxide is a polysilicon-containing material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use non-doped polysilicon as the planarizing material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 16 and 17, Enders et al. disclose the use of various materials for the conductive layers including the use of titanium, titanium nitride, titanium silicide and tungsten among others to form contacts and interconnections. It is an inherent property of these materials to be highly resistant to dopant diffusion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use any of the above recited metals as used by Enders et al. in the contacts and metal layers as the interconnect material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 28, Enders et al. discloses in Figs. 2S and 5C a field effect transistor that comprises a p-type gate portion 56p and an n-type gate portion 56n on a vertical single crystal Si semiconductor body 54a; the p-type and n-type gate portions are composed of polysilicon; a metal interconnect 1 between the p-type gate portion 56p and the n-type gate portion 56n; and a planarizing structure (110 and metal 1)

above the interconnect 1; Enders et al. further discloses in Figs. 2S and 5C a field effect transistor that comprises a patterned stack including at least a vertical semiconductor body 54a having sidewalls 52 located on an upper surface of a substrate; a gate dielectric 52 located on the sidewalls of the vertical semiconductor body; a p-type gate portion 56p located on one side of the vertical semiconductor body and an n-type gate portion 56n located on an opposing side of the vertical semiconductor body 54a, the gate portions located on the upper surface of the substrate and are separated from the vertical semiconductor body 54a by the gate dielectric, and an interconnect located at least over the p-type gate portion and the n-type gate portion and a planarizing structure (110 and metal 1) above the interconnect 1.

Regarding the feature of the planarizing structure being a doped polysilicon structure, Enders et al. discloses that the p-type gate portion and the n-type gate portion are composed of a polysilicon containing material. Enders et al. further discloses that the planarizing structure comprises silicon oxide. Thus, although a different material, silicon oxide is a polysilicon-containing material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use doped or non-doped polysilicon as the planarizing material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding the feature of the interconnect being a metal silicide interconnect, Enders et al. disclose the use of various materials for the conductive layers including the

use of titanium, titanium nitride, titanium silicide and tungsten among others to form contacts and interconnections. It is an inherent property of these materials to be highly resistant to dopant diffusion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use metal silicide as used by Enders et al. in the contacts and metal layers as the interconnect material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

*Response to Arguments*

9. Applicant's arguments filed 5/2/03 have been fully considered but they are not persuasive.

With regards to applicant's arguments directed to the newly amended claims, the newly added features are addressed above in the rejections.

With regards to applicant's argument that in Enders et al. the transistors are formed into trenches that are located below an upper surface of a semiconductor body, and that Enders et al do not disclose applicant's patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of the substrate, it is noted that although the process starts by forming trenches in the substrate, the final structure that is shown in Fig. 5C clearly shows a patterned stack including at least a vertical semiconductor body 54a having sidewalls located on an upper surface of a substrate 14, it is further noted that as the claims are directed to the

device and not to the method of making the device, and that the final structure of Enders et al. discloses the semiconductor body 54a on an upper surface of the substrate, that the structure of Enders et al. discloses the claimed feature.

With regards to Enders et al. not teaching an asymmetric FET, it is noted that the phrase "asymmetric FET" is only recited on the preamble and has not been given any patentable weight, since Enders et al teach the described features in the claims.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP  
July 10, 2003

S.